**EE 414 Lab 5 Report:**

**DC Bias Regulator**

**Due: November 5, 2021**

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**Introduction**

For our fifth lab in EE414, we are designing a DC Bias Regulator. The purpose of designing one is to set the correct DC collector voltage and current for the RF device.

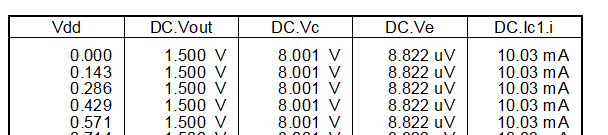
**Part 1: Regulator Design**

- Resistor values calculation of the regulator circuit

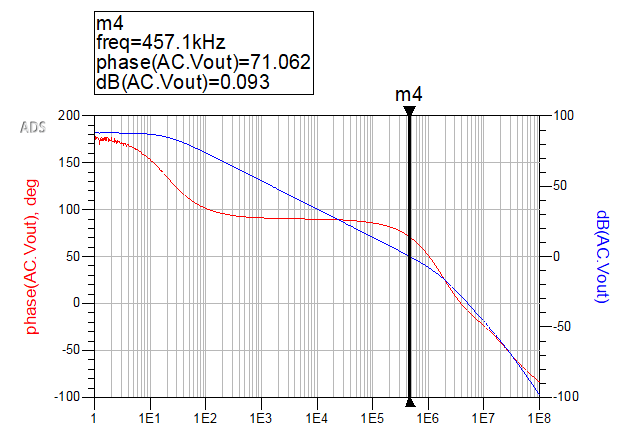
B = ((VCE/VREF) - 1 ) B^-1 = RP/(RS+RP)

| VCE = 8V | Vref = 1.43V | B = 4.594 | Rp = 220K | Rs = 1M |
| --- | --- | --- | --- | --- |

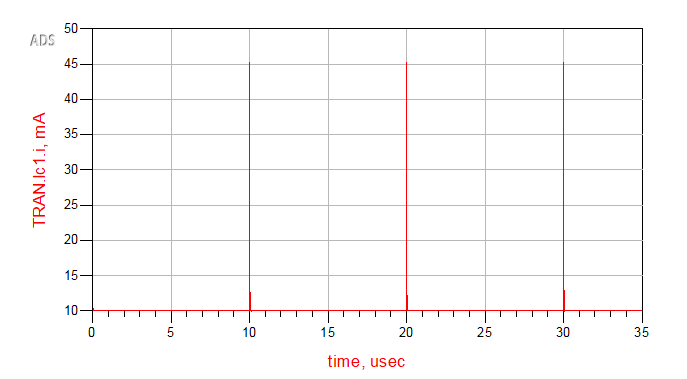
- DC simulation showing that regulator is providing correct bias



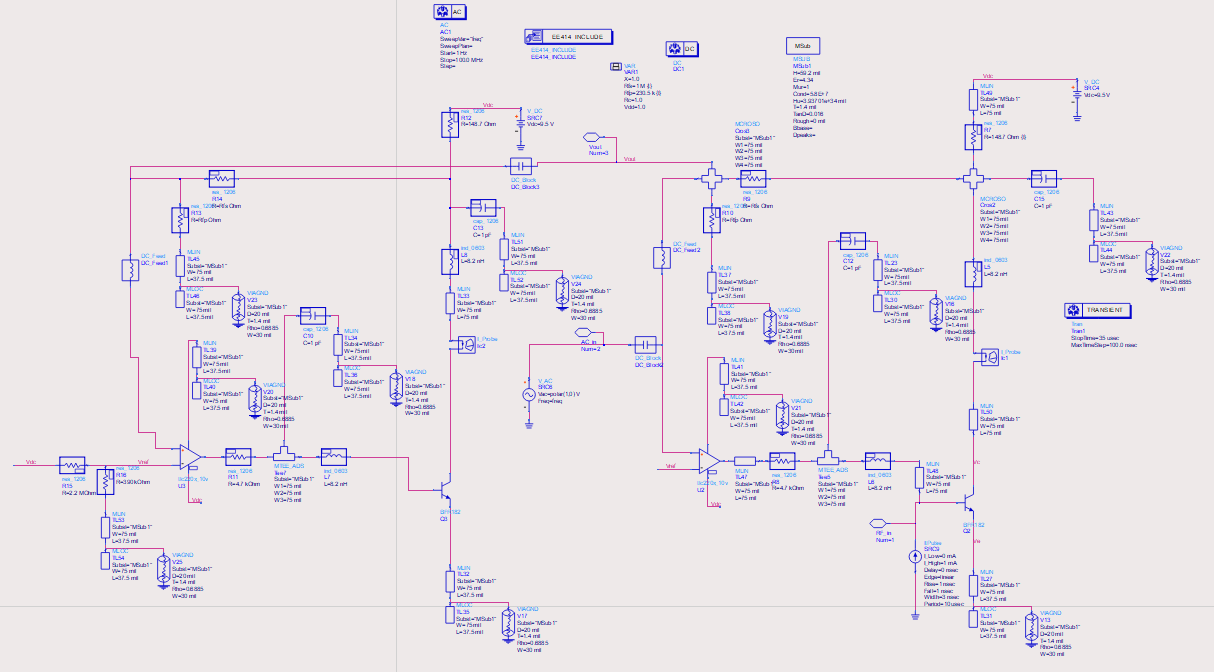
- AC stability simulation showing phase margin > 60 degrees



- Transient simulation showing IC recovery after a step disturbance

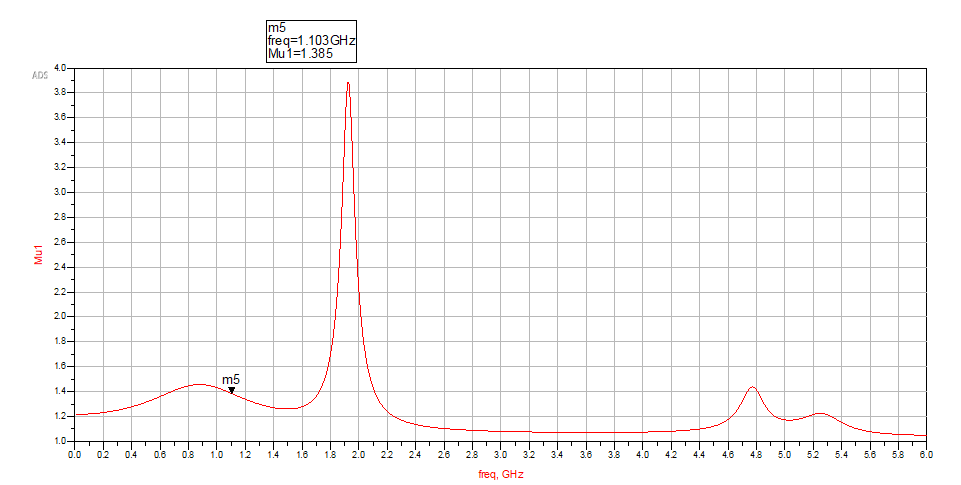
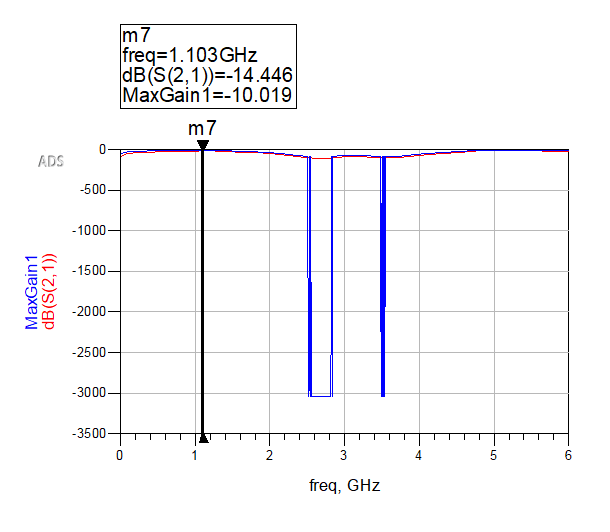


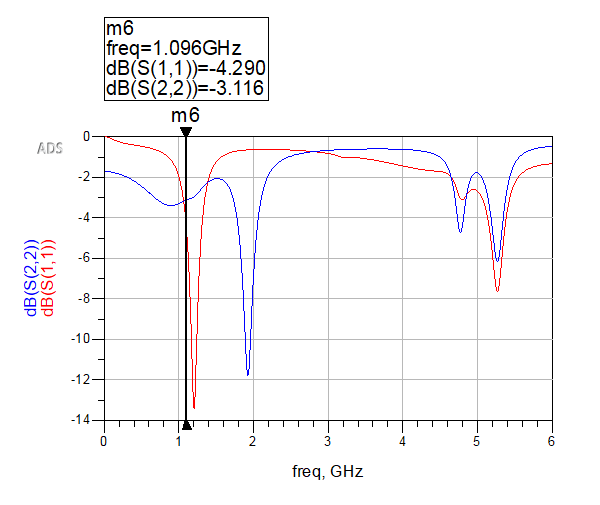
- Full schematics of the regulator with non-ideal components

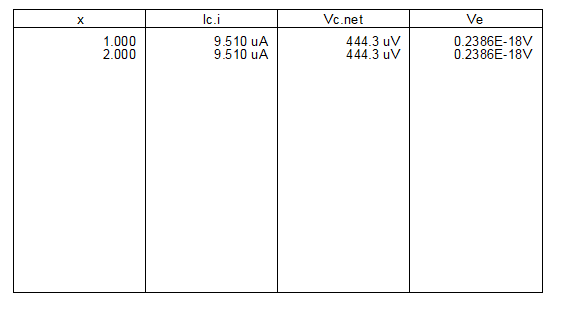


**Part 2: Regulator Biased Amplifier**

* S-parameter simulation:







**Part 3: Regulator Biased Oscillator**

* Harmonic balance simulations:

